S/N Unknown PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jason M. Howard et al.	Examiner: Unknown	
Serial No.:	Unknown	Group Art Unit: Unknown	
Filed:	Herewith	Docket: 884.584US1	
Title:	MULTI-THREADED MULTIPLY ACCUMULATOR		

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5/8/02

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of the 1449 form, initialed by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Under 37 C.F.R. §1.97(b)(3), it is believed that no fee or certificate is required with this Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Account No. 19-0743.

The Examiner is invited to contact the Applicants' Representatives at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

JASON M. HOWARD ET AL.

By their Representatives,

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"Express Mail" mailing label number: EV019077236US
Date of Deposit: February 8, 2002
This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to The Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Form 1449*	Atty. Docket No.: 884.584US1	Serial No. Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Jason M. Howard et al.	
	Filing Date: Herewith	Group: Unknown

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
_____	5,612,632	03/18/1997	Mahant-Shetti et al.	326	46	11/29/94
_____	5,764,089	06/09/1998	Partovi et al.	327	200	08/30/96
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_____	5,900,759	05/04/1999	Tam	327	201	06/26/97
_____	6,242,952	06/05/2001	Bosshart et al.	326	98	09/24/99
_____	6,304,123	10/16/2001	Bosshart	327	212	08/02/00

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
_____	01-206717	08/18/1989	Japan	H03K	3/37	X (abstract)	

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	
	Anonymous, "Power Saving Latch", IBM Technical Disclosure Bulletin, 39, 65-66, (Apr. 1, 1996)
	Beaumont-Smith, A., et al., "Reduced Latency IEEE Floating-Point Standard Adder Architectures", Proceedings of the 14th IEEE Symposium on Computer Arithmetic, 8 pgs., (1998)
	Elguibaly, F., "A Fast Parallel Multiplier-Accumulator Using the Modified Booth Algorithm", IEEE Transactions on Circuits and Systems -- II : Analog and Digital Signal Processing, 47 (9), pp. 902-908, (Sept. 2000)
	Even, G., et al., "On the Design of IEEE Compliant Floating Point Units", IEEE Transactions on Computers, Vol. 49, 398-413, (May 2000)
	Goto, G., et al., "A 54 X 54-b Regularly Structured Tree Multiplier", IEEE Journal of Solid-State Circuits, Vol. 27, 1229-1236, (Sept. 1992)
	Hokenek, E., et al., "Second-Generation RISC Floating Point with Multiply - Add Fused", IEEE Journal of Solid-State Circuits, 25 (5), pp. 1207-1213, (1990)
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	Klass, F., "Semi-Dynamic and Dynamic Flip-Flops with Embedded Logic", Proceedings of the Symposium on VLSI Circuits, Digest of Technical Papers, Honolulu, HI, IEEE Circuits Soc. Japan Soc. Appl. Phys. Inst. Electron., Inf. & Commun. Eng. Japan, pp. 108-9, (1998)

Examiner	Date Considered

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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OTHER DOCUMENTS

**Examiner Initial	(Including Author, Title, Date, Pertinent Pages, Etc.)
	Lee, K.T., et al., "1 GHz Leading Zero Anticipator Using Independent Sign-Bit Determination Logic", 2000 Symposium on VLSI Circuits Digest of Technical Papers, 194-195, (2000)
	Luo, Z., et al., "Accelerating Pipelined Integar and Floating-Point Accumulations in Configurable Hardware with Delayed Addition Techniques", IEEE Transactions on Computers, 49 (3), 208-218, (March 2000)
	Panneerselvam, G., et al., "Multiply-Add Fused Risc Architectures for DSP Applications", IEEE Pac Rim, pp. 108-111, (1993)
	Partovi, H., et al., "Flow-Through Latch and Edge-Triggered Flip-Flop Hybrid Elements", Proceedings of the IEEE International Solid-State Circuits Conference, Digest of Technical Papers and Slide Supplement, NexGen Inc., Milpitas, CA, 40 pgs., (1996)

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